Building a Battery Operated Auto Ranging DVM with the ICL7106

Application Note **AN046**

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Introduction

In the field of DVM design, three areas are being addressed with vigor: size, power dissipation, and novelty. The handheld portable multimeter has gained in popularity since low power dissipation devices enabled battery operation, LSI A/D converters reduced IC count, and novelties such as conductance, automatic range scaling, and calculating were included to entice the user.

This application note describes a technique for auto-ranging a battery operated DVM suitable for panel meter applications. Also, circuit ideas will be presented for conductance and resistance measurement, 9V battery and 5V supply operations, and current measurement.

Auto Ranging Circuitry

The control signals necessary for auto-ranging are over-range, under-range, and clock. The over-range and under-range inputs control the direction of a scale shift, becoming active at the completion of an invalid conversion and remaining active until a valid conversion occurs. The clock input controls the timing of a scale shift. This signal should occur only once per conversion cycle, during a time window which will not upset an ongoing conversion and must be disabled after valid conversions.

In the circuit of Figure 1, inverted over-range ($\overline{O/R}$) and under-range ($\overline{U/R}$) are generated by detecting the display reading. The ICL7106 turns the most significant digit on and blanks the rest to indicate an over-range. An under-range occurs if the display reads less than 0100. R_1C_1 and R_2C_2 are required to deglitch $\overline{O/R}$ and $\overline{U/R}$.

The next step in the logic disables $\overline{O/R}$ and $\overline{U/R}$ prior to shifting into nonexistent ranges. $\overline{O/R}$ is disabled when in the 200V range, while $\overline{U/R}$ is disabled when in the 200mV range.

The next level of gating disables the clock if the conditions are as described above and a valid conversion state exists. Clock is enabled only when a range shift is called for and there exists a valid range to shift into.

The CD4029 is a four bit up/down counter, used as a register to hold the present state and as a counter to shift the scale as directed by the control inputs. The CD4028 is a BCD to decimal decoder interfacing the CD4029 and ladder switches. An additional exclusive OR gate package is added to drive the appropriate decimal point.

Input Divider Network

A simplified drawing of the divider network is shown in Figure 2. This configuration was chosen for simplicity and implementation using analog switches. The low leakage ID101s are used for input protection, and the second set of switches to IN LO reduces the net error due to switch resistance. This can be seen calculating IN HI and IN LO voltages for the two equivalent circuits.

For equivalent circuit A,

$$V_{MEAS} = V_{IN\ HI} = \left(\frac{R_S + R/K}{R_S + R + R/K}\right) V_{IN} \quad \text{(EQ. 1)}$$

where R_S = switch resistance, R = input resistance (1MΩ), and 1 + K is the desired divider ratio.

Ideally V_{INHI} should be

$$V_{IDEAL} = \left(\frac{R/K}{R/K + R}\right) V_{IN} = \left(\frac{1}{1+K}\right) V_{IN} \quad \text{(EQ. 2)}$$

Therefore the percent error is:

$$\left[\frac{\text{Ideal} - \text{Actual}}{\text{Ideal}}\right] 100, \quad \text{(EQ. 3)}$$

$$\text{or } \left(1 - (1+K)\frac{R_S + R/K}{R_S + R/K + R}\right) 100 \quad \text{(EQ. 4)}$$

The worst case error occurs at (1+K) = 1000. For this example, the error due to a 1kW switch resistance is 99.7%.

IN HI for equivalent circuit B is the same as Equation 1. However, IN LO for circuit B is:

$$\left(\frac{R_S}{R_S + R + R/K}\right) V_{IN}, \quad \text{(EQ. 5)}$$

and combining Equations (1) and (5)

$$V_{MEAS} = V_{INHI} - V_{INLO} = \left(\frac{R/K}{R_S + R + R/K}\right) V_{IN} \quad \text{(EQ. 6)}$$

The percent error is equal to:

$$\left(1 - (1+K)\frac{R/K}{R + R_S + R/K}\right) 100 \quad \text{(EQ. 7)}$$

Using the same values for R_S, (1+K), and R, the worst case error is 0.1%. This error can be further improved if lower $r_{DS(ON)}$ switches are used. From the results calculated above, the worst case conversion error due to switch resistance will be one count of the least significant digit for a full scale input, and a slight adjustment to R itself will correct the remaining error on all scales.

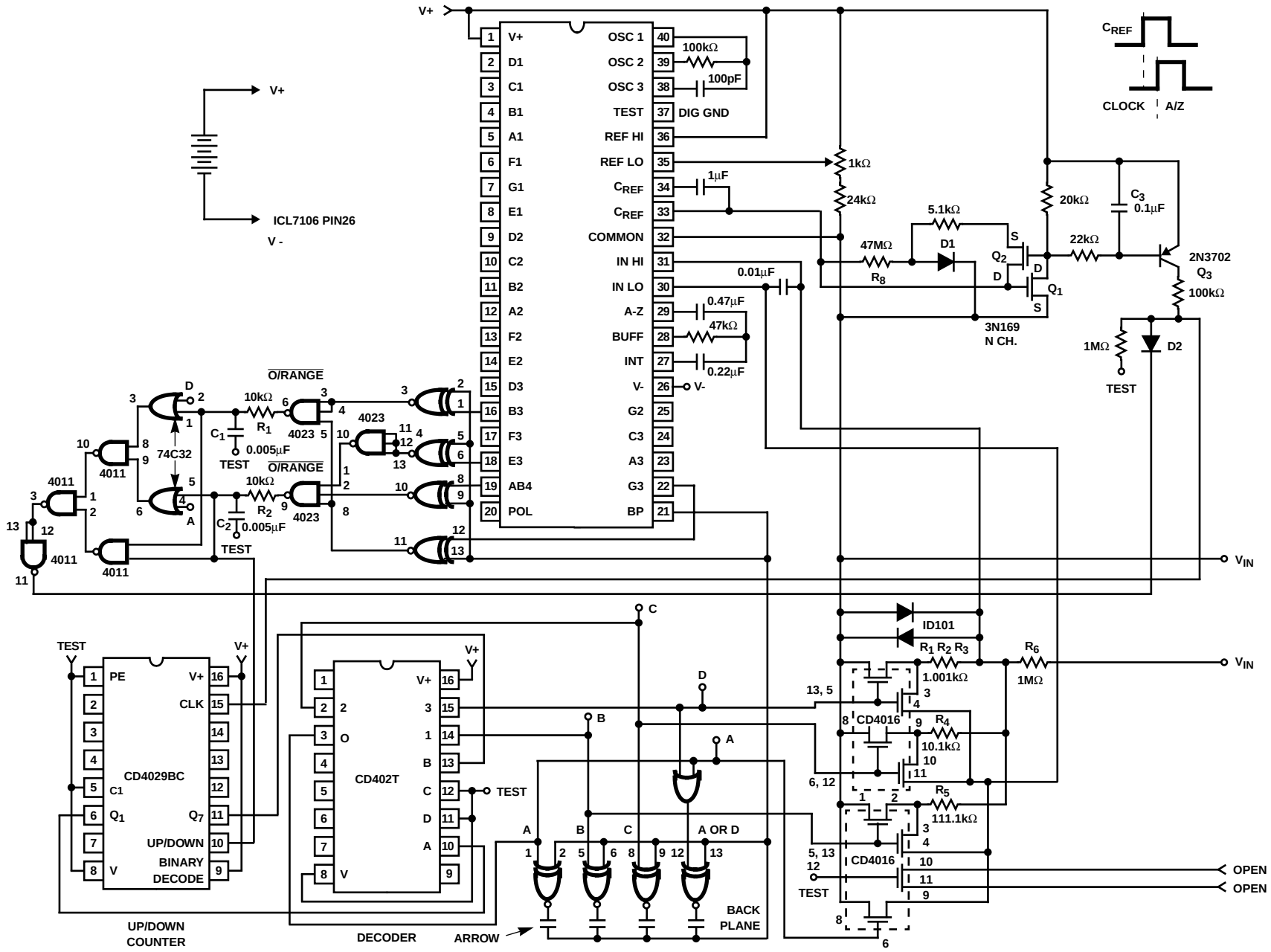

FIGURE 1. AUTO RANGING CIRCUITRY

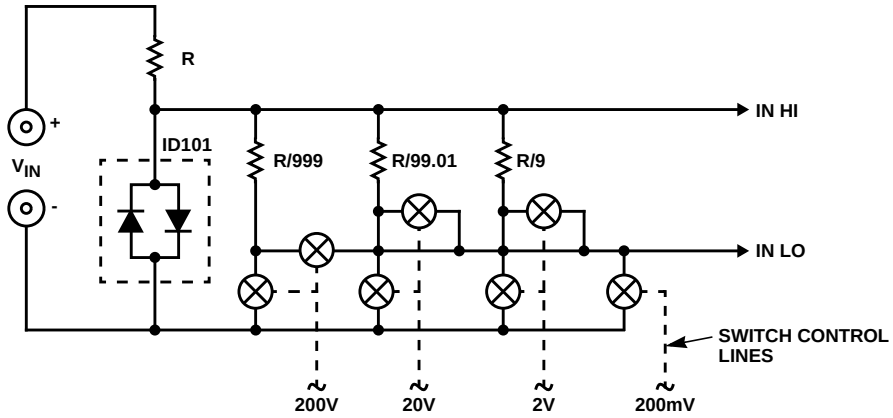

FIGURE 2A.

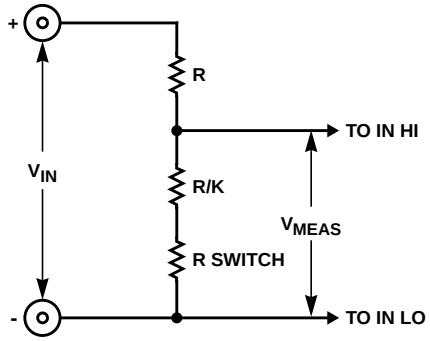

FIGURE 2B. EQUIVALENT CIRCUIT A (SWITCHES TO IN LO REMOVED)

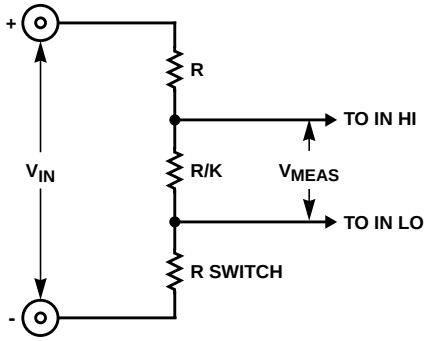

FIGURE 2C. EQUIVALENT CIRCUIT B (SWITCHES TO IN LO INCLUDED)

FIGURE 2. INPUT DIVIDER NETWORK

Ranging Clock Circuit

Two N-Channel MOSFETs, a PNP transistor and a handful of passive components combine to generate the clock signal used to gate the auto-ranging logic. A closer look at the inner workings of the ICL7106 will help clarify the discussion of this circuit. The analog section of the ICL7106 is shown in Figure 3.

It can be shown that C_{REF} low (pin 33 of ICL7106) will sit at $-V_{REF}$ for DE+ and at common for DE-, with DE+ designating the deintegrate phase for a positive input signal and DE- referring to a negative input signal. During the auto-zero phase, C_{REF} low is tied to an external reference through pin 35, which in Figure 1 is V_{REF} below the positive supply. The net result is that C_{REF} low is above COMMON during auto-zero, is left to float during signal integrate, and is at or below COMMON during deintegrate. R_8 and D_1 are added externally to pull C_{REF} to COMMON during integrate, with Q_2 and R_1 included to speed this action. The signal at C_{REF} low is now a square wave that is high during auto-zero and low at all other times. Q_1 and Q_3 amplify and level shift this waveform for logic level compatibility. This clock signal is gated through D_2 and controls the timing of the auto-ranging circuitry. C_3 is added to delay the clock, eliminating disparity with $\overline{O/R}$ and $\overline{U/R}$ (see Figure 4 for timing diagram).

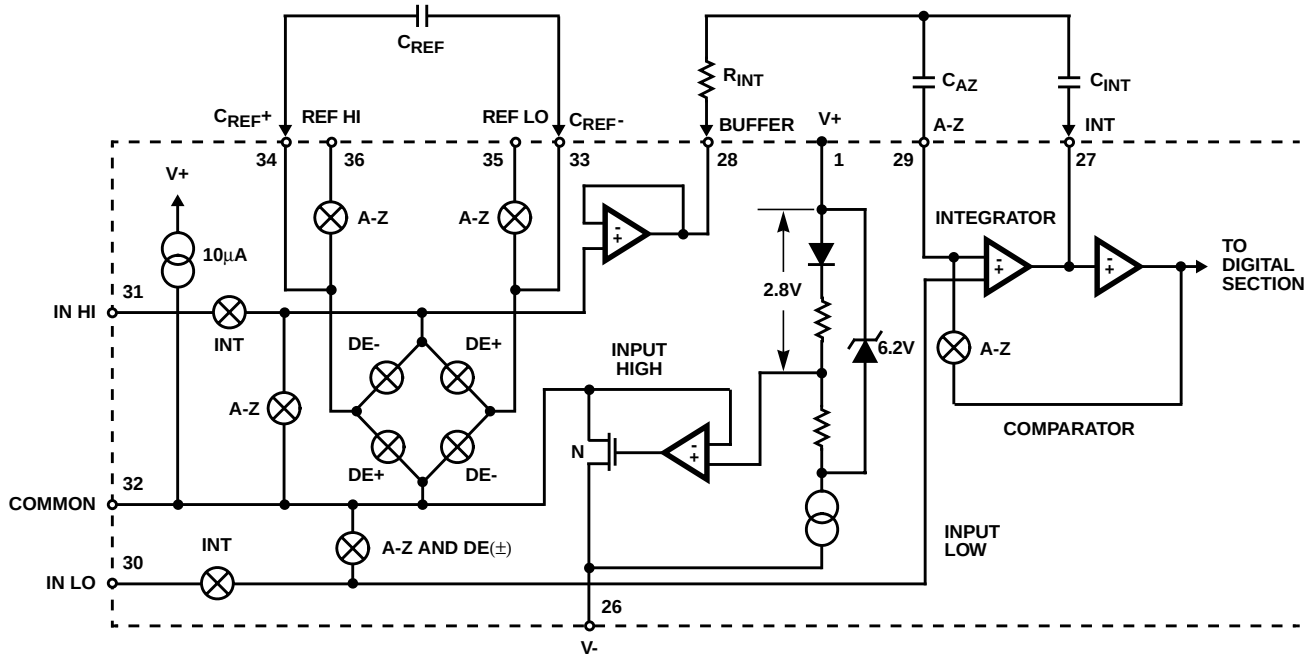

FIGURE 3. ANALOG SECTION OF ICL7106

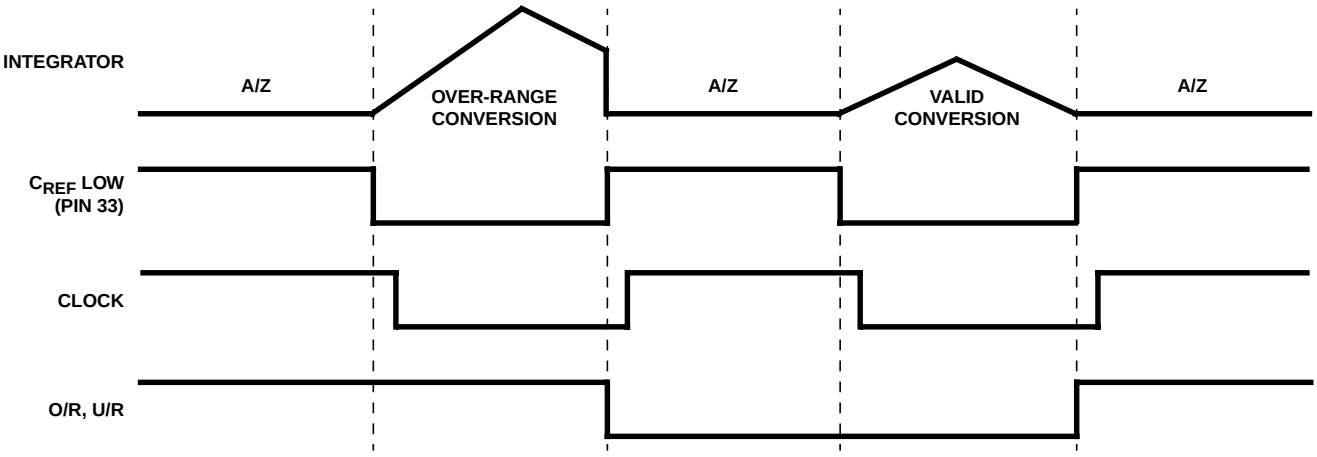

FIGURE 4. TIMING DIAGRAM

Supply Requirements

The circuit of Figure 1 operates on a standard 9V transistor battery. CMOS logic and a CMOS A/D converter (ICL7106) are used to extend battery life; the approximate power drain for this circuit is 8mW. The circuit in Figure 5 can also be added to detect low supply voltage.

The circuit of Figure 6 can be used to generate ±5V from a single 5V supply. The ICL7660 is a voltage converter which takes a 5V input and produces a -5V output. With respect to common mode signals, the circuit of Figure 1 will have infinite common mode handling capability if operated from a floating 9V battery. However, if powered by a fixed supply such as in Figure 6, the common mode capability of the converter will be limited to approximately ±2V, if COMMON is disconnected from $-V_{IN}$.

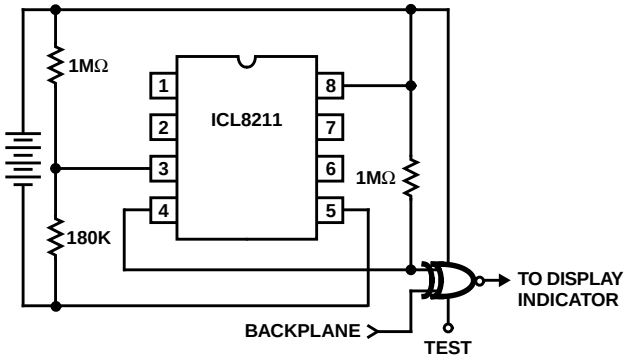

FIGURE 5. LOW VOLTAGE DETECTOR

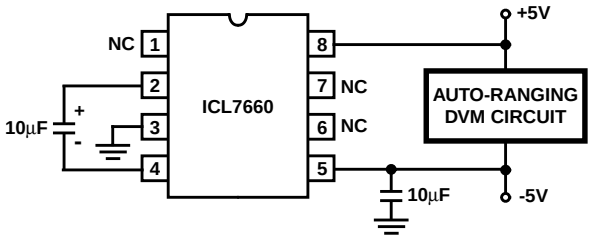

FIGURE 6. GENERATING ±5V FROM +5V

Resistance, Transconductance and Current Circuits

The purpose of this section is to show the simplicity of measuring transconductance (1/R) and resistance with the ICL7106. The circuit of Figure 7 requires only one precision resistor per decade range of interest. The conversion output is described by the formula:

$$\left(\frac{R_X}{R_{STD}}\right) 1000 \qquad \text{(EQ. 8)}$$

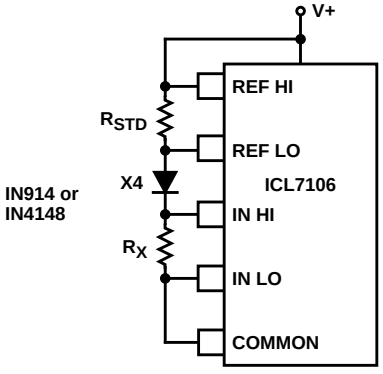

FIGURE 7. TRANSCONDUCTANCE AND RESISTANCE MEASUREMENT

For transconductance measurement, merely switch R_{STD} and R_X. This scheme makes the measurement of large resistors, in conductance form, convenient and easy. This is also convenient for leakage measurements.

A simple current meter can be built using the circuit of Figure 8. The low leakage of the ICL7106 (10pA/max) makes possible the measurement of currents in the mid pico-Amp range. However, the switch leakage current will limit the accuracy of the resistor network and may degrade converter resolution.

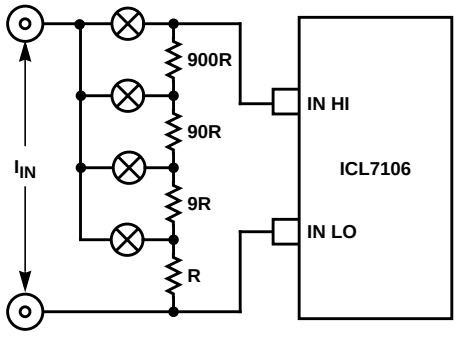

FIGURE 8. CURRENT METER

Using the ICL7126 and ICL7107

With a few modifications, the circuit of Figure 1 can easily be adapted for use with either the low power ICL7126 or the ICL7107. Using the ICL7126 simply requires a change in the values of the integrating and auto-zero components. Refer to the ICL7126 data sheet for details.

The ICL7107 is an LED version of the ICL7106, and is a bit trickier to use in this application. First the over-range/under-range logic must be changed slightly. Simply replace the quad exclusive-NOR with an LM339; connect the outputs, as before, to the CD4023 triple 3-input NAND. Second, the ICL7107 requires +5V and -5V rather than the +9V battery used in Figure 1. If battery operation is desired, the negative supply can be derived from 4 Ni-Cad cells in series and an ICL7660 (see Figure 9). Note that both supplies float with respect to the input terminals. (Logic supplies are V+ and DIG. GND.)

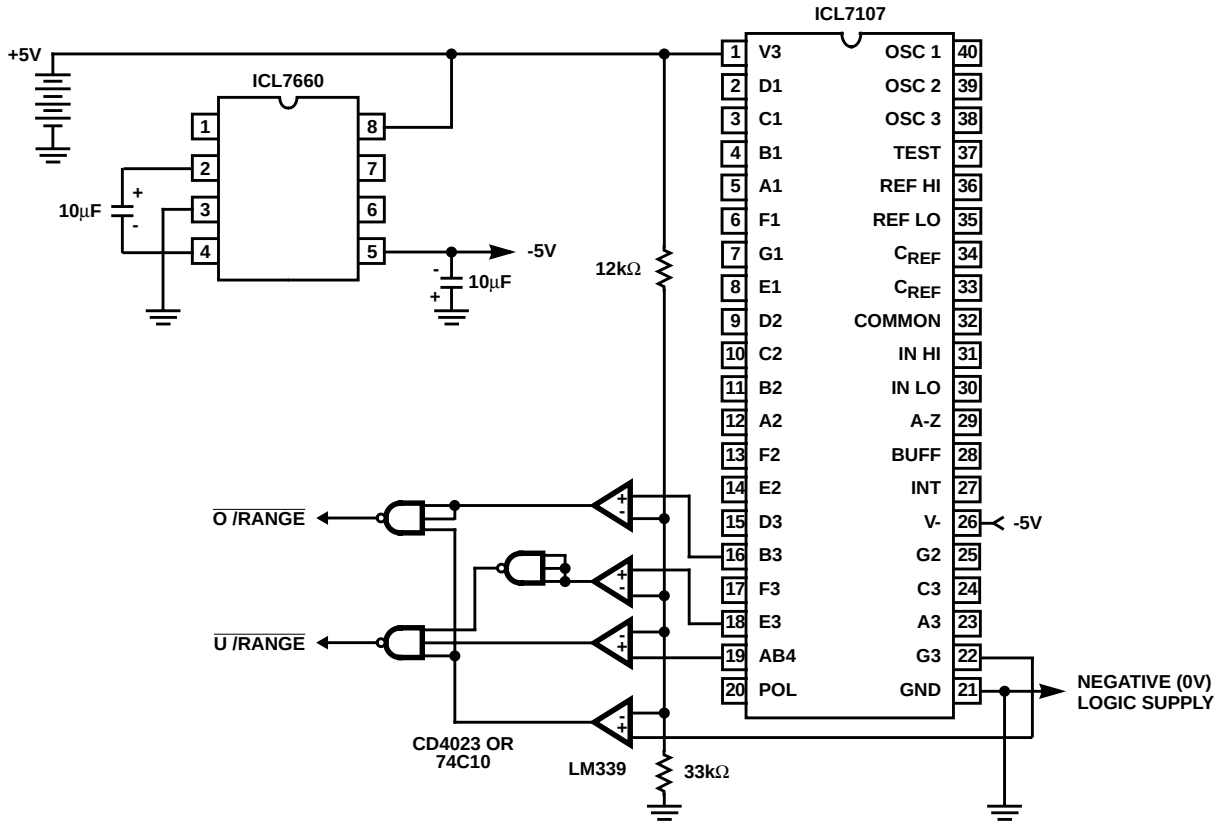

FIGURE 9. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM ICL7107 OUTPUTS. THE LM339 IS REQUIRED TO ENSURE LOGIC COMPATIBILITY WITH HEAVY DISPLAY LOADING

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